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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
LI, AIMEE J	

ART UNIT	PAPER NUMBER
2183	

DATE MAILED: 12/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/704,467	ROTH ET AL.	
	Examin r	Art Unit	
	Aimee J Li	2183	

-- The MAILING DATE of this communication app ars on the cover sh et with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-9,11-16,18-21 and 23-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5-9,11-16,18-21 and 23-31* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1, 3, 5-9, 11-16, 18-21, 23-30, and new claim 31 have been considered. Claims 1, 3, 5-9, 16, 19, 23-24, 26, and 30 have been amended as per Applicant's request. Claims 2, 4, 10, 17, and 22 have been cancelled as per Applicant's request. New claim 31 has been added as per Applicant's request.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 9, 15, 16, 20, 21, 24, 26, 27, 29, 30, and 31 are rejected under 35 U.S.C. 102(b) as being taught by Deao et al., U.S. Patent Number 5,970,241 (herein referred to as Deao).

4. Referring to claim 9, Deao has taught a method of providing instructions to a processor, the method comprising:

a. Loading a plurality of instructions into an emulation instruction register (Deao column 8, lines 28-37 and Figure 1). In regards to Deao, the program memory, element 23 in Figure 1, contains the instructions and, as stated by Deao, it is a design choice for location and type, i.e. registers or cache.

b. Receiving a run-test idle state signal (Deao column 5, lines 12-38);

c. Providing the plurality of instructions to the processor (Deao column 7, line 65 to column 8, line 21 and Figure 1); and

d. Processing the plurality of instructions without receiving another run-test idle state signal (Deao column 5, lines 12-38).

5. Referring to claim 16, Deao has taught a processor comprising:

a. A test interface (Deao Abstract; column 4, lines 42-62; column 7, lines 49-51; column 8, lines 22-27; and Figure 1);

b. An emulation instruction register adapted to store a plurality of emulation instructions received from the test interface (Deao Abstract; column 4, lines 42-62; column 7, lines 49-51; column 8, lines 22-37 and Figure 1). In regards to Deao, the program memory, element 23 in Figure 1, contains the instructions and, as stated by Deao, it is a design choice for location and type, i.e. registers or cache.

c. Emulation control logic adapted to control a flow of the plurality of emulation instructions to a processor pipeline following detection of a single run-test idle state (Deao column 5, lines 12-38); and

d. A decoder to receive the plurality of instructions for processing (Deao column 20, line 58 to column 21, line 2; Table 15; and Figure 11).

6. Referring to claims 15 and 20, Deao has taught providing the plurality of instructions to a digital signal processor (Deao column 15, lines 28-51; column 20, line 58 to column 21, line 2; Table 15; Figure 9; and Figure 11).

7. Referring to claim 21, Deao has taught an apparatus, including operating instructions residing on a machine-readable storage medium, for use in a device to handle a plurality of emulation instructions, the operating instructions causing the device to:

a. Load the plurality of emulation instructions into a single emulation instruction register (Deao column 8, lines 28-37 and Figure 1). In regards to Deao, the program memory, element 23 in Figure 1, contains the instructions and, as stated by Deao, it is a design choice for location and type, i.e. registers or cache.

b. Enter a run-test idle state (Deao column 5, lines 12-38);

c. Provide the plurality of emulation instructions to a processor (Deao column 15, lines 28-51; column 20, line 58 to column 21, line 2; Table 15; Figure 9; and Figure 11); and

d. Process the plurality of emulation instructions (Deao column 15, lines 28-51; column 20, line 58 to column 21, line 2; Table 15; Figure 9; and Figure 11).

8. Referring to claim 24, Deao has taught scanning instructions from an in-circuit emulator (ICE) to the test interface, the test interface comprising a Joint Test Action Group (JTAG) interface (Deao Abstract; column 4, lines 11-18 and 42-62; column 7, lines 49-51; column 8, lines 22-27; column 54, lines 25-38; Figure 1; and Figure 35).

9. Referring to claim 26, Deao has taught wherein the emulation_instruction register comprises first and second registers (Deao Abstract; column 4, lines 42-62; column 7, lines 49-51; column 8, lines 22-37 and Figure 1). In regards to Deao, the program memory, element 23 in Figure 1, contains the instructions and, as stated by Deao, it is a design choice for location and type, i.e. registers or cache.

10. Referring to claim 27, Deao has taught wherein the emulation control logic comprises a state machine (Deao column 37, lines 39-53 and Figure 22).

11. Referring to claim 29, Deao has taught an in-circuit emulator to monitor operations of the processor (Deao column 3, line 53 to column 4, line 41 and column 8, lines 18-27).

12. Referring to claim 30, Deao has taught executing at least one of the plurality of instructions to monitor operation of the processor (Deao column 3, line 53 to column 4, line 41 and column 8, lines 18-27).

13. Referring to claim 31, Deao has taught performing a debugging operation using the first and second instructions (Deao column 3, line 53 to column 4, line 41 and column 8, lines 18-27).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. Claims 1-8, 11-15, 18-19, 23, and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Deao et al., U.S. Patent Number 5,970,241 (herein referred to as Deao) in view of O'Connor, U.S. Patent Number 5,848,288 (herein referred to as O'Connor).

16. Referring to claim 1, Deao has taught a method comprising:

a. Receiving a plurality of instructions from a test interface (Deao Abstract; column 4, lines 42-62; column 7, lines 49-51; column 8, lines 22-27; and Figure 1);

b. Loading the plurality of instructions into an emulation instruction register (Deao column 8, lines 28-37 and Figure 1). In regards to Deao, the program memory, element 23 in Figure 1, contains the instructions and, as stated by Deao, it is a design choice for location and type, i.e. registers or cache.

c. Receiving a plurality of instructions from the emulation instruction register (Deao column 7, line 65 to column 8, line 21 and Figure 1);

d. Determining a validity of a first instruction of the plurality of instructions (Deao column 15, lines 28-51 and Figure 9). In regards to Deao, the instruction is only valid when it is 8 instructions wide.

e. Providing the first instruction to a decoder of the processor if the first instruction is valid (Deao column 20, line 58 to column 21, line 2; Table 15; and Figure 11);

f. Without receiving a run-test idle state signal, determining a validity of a second instruction of the plurality of instructions (Deao column 15, lines 28-51; column 20, line 58 to column 21, line 2; Table 15; Figure 9; and Figure 11). In regards to Deao, the instruction is only valid when it is 8 instructions wide.

g. Providing the second instruction to the decoder if the second instruction is valid (Deao column 20, line 58 to column 21, line 2; Table 15; and Figure 11).

17. Deao has not explicitly taught determining a validity of an instruction of the plurality of instructions by reading width bits in the instruction. However, Deao has taught that there must be eight instructions in a fetch packet for the VLIW instructions to match the eight instruction units (Deao column 15, lines 28-51 and Figure 9). O'Connor has taught checking the validity of a VLIW instruction by looking for a bit indicating the end of a VLIW instruction (O'Connor Abstract; column 2, line 6-19; column 2, line 53 to column 3, line 9; and Figure 1). In regards to O'Connor, the end of bundle bits are like the width bits, since it shows when the VLIW instruction has reached its maximum size, i.e. width, in regards to the number of subinstructions found in an individual fetch packet. A person of ordinary skill in the art at the time the invention

was made would have recognized that the end of bundle bits allows compatibility between various VLIW systems and eliminate the slower clock cycles needed for dependency checking (O'Connor column 1, lines 36-45 and column 1, line 62 to column 2, line 2), thereby increasing compatibility and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the end of bundle bits of O'Connor in the device of Deao to increase compatibility and speed.

18. Referring to claim 3, Deao has taught storing the plurality of instructions in the emulation instruction register in subsequent clock cycles (Deao column 8, lines 28-37; column 20, line 58 to column 21, line 2; Table 15; Figure 1; and Figure 11). In regards to Deao, the program memory, element 23 in Figure 1, contains the instructions and, as stated by Deao, it is a design choice for location and type, i.e. registers or cache.

19. Referring to claim 5, Deao has taught loading the plurality of instructions in parallel into the emulation instruction register (Deao column 8, lines 28-37; column 20, line 58 to column 21, line 2; Table 15; Figure 1; and Figure 11).

20. Referring to claim 6, Deao has taught providing the second instruction to the decoder after the first instruction is completed (Deao column 15, lines 28-51; column 20, line 58 to column 21, line 2; Table 15; Figure 9; and Figure 11).

21. Referring to claim 7, Deao has taught providing the plurality of instructions to the decoder after a first run-test idle state without entering into a second run-test idle state (Deao column 5, lines 12-38).

22. Referring to claim 8, Deao has taught providing the first and second instructions to a digital signal processor (Deao column 15, lines 28-51; column 20, line 58 to column 21, line 2; Table 15; Figure 9; and Figure 11).

23. Referring to claims 11-15, 18-19, 23, and 25, Deao has not explicitly taught

a. Determining a validity of each of the plurality of instructions before processing by reading bits in each instruction indicating a width of the instruction (Applicant's claims 11, 18, and 23).

b. Aborting processing of any invalid instructions and loading a next instruction of the plurality of instructions from the instruction register (Applicant's claims 12, 18, and 25).

c. Loading a next instruction of the plurality of instructions from the instruction register if a no-operation instruction is loaded (Applicant's claims 13 and 19).

d. Providing the plurality of instructions to the processor a plurality of times without reloading the instruction register (Applicant's claim 14).

24. However, Deao has taught that there must be eight instructions in a fetch packet for the VLIW instructions to match the eight instruction units (Deao column 15, lines 28-51 and Figure 9). O'Connor has taught

a. Determining a validity of each of the plurality of instructions before processing by reading bits in each instruction indicating a width of the instruction (Applicant's claim 11) (O'Connor Abstract; column 2, line 6-19; column 2, line 53 to column 3, line 9; and Figure 1).

b. Aborting processing of any invalid instructions and loading a next instruction of the plurality of instructions from the instruction register (Applicant's claim 12) (O'Connor Abstract; column 2, line 6-19; column 2, line 53 to column 3, line 9; and Figure 1).

c. Loading a next instruction of the plurality of instructions from the instruction register if a no-operation instruction is loaded (Applicant's claim 13) (O'Connor Abstract; column 2, line 6-19; column 2, line 53 to column 3, line 9; and Figure 1).

d. Providing the plurality of instructions to the processor a plurality of times without reloading the instruction register (Applicant's claim 14) (O'Connor Abstract; column 2, line 6-19; column 2, line 53 to column 3, line 9; and Figure 1).

25. In regards to O'Connor, the end of bundle bits are like the width bits, since it shows when the VLIW instruction has reached its maximum size, i.e. width, in regards to the number of subinstructions found in an individual fetch packet. A person of ordinary skill in the art at the time the invention was made would have recognized that the end of bundle bits allows compatibility between various VLIW systems and eliminate the slower clock cycles needed for dependency checking (O'Connor column 1, lines 36-45 and column 1, line 62 to column 2, line 2), thereby increasing compatibility and speed. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the end of bundle bits of O'Connor in the device of Deao to increase compatibility and speed.

26. Claim 28 is rejected under 35 U.S.C. 103(a) as being unpatentable over Deao et al., U.S. Patent Number 5,970,241 (herein referred to as Deao) in view of Dowling, U.S. Patent Number

6,170,051 (herein referred to as Dowling). Deao has not taught a multiplexer to select between an instruction for the plurality of instructions to send to the processor pipeline. Dowling has taught a multiplexer to select between an instruction for the plurality of instructions to send to the processor pipeline (Dowling column 12, lines 17-21 and Figure 4, element 440). A person of ordinary skill in the art at the time the invention was made would have recognized that the multiplexer determines which instruction stream each operational unit receives (Dowling column 12, lines 17-21), thereby ensuring that the execution units operate the correct instruction. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the multiplexer of Dowling in the device of Deao to ensure correct instruction operation.

Conclusion

27. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure as follows. Applicant is reminded that in amending in response to a rejection of claims, the patentable novelty must be clearly shown in view of the state of the art disclosed by the references cited and the objections made. Applicant must also show how the amendments avoid such references and objections. See 37 CFR § 1.111(c).

a. Edington et al., U.S. Patent Number 5,530,804, has taught a superscalar processor with debug modes from an in-circuit emulator.

b. Baeg, U.S. Patent Number 5,812,562, has taught a JTAG emulation debug port for a digital signal processor.

28. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Aimee J Li whose telephone number is (571) 272-4169. The examiner can normally be reached on M-T 7:30am-5:00pm.

29. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

30. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AJL
Aimee J. Li
14 December 2004

RICHARD L. ELLIS
PRIMARY EXAMINER